HIGH TOLERANCE TCR BALANCED HIGH CURRENT RESISTOR FOR RF CMOS AND RF SIGE BICMOS APPLICATIONS AND CADENCED BASED HIERARCHICAL PARAMETERIZED CELL DESIGN KIT WITH TUNABLE TCR AND ESD RESISTOR BALLASTING FEATURE

RELATED APPLICATIONS

This application is a divisional of U.S. application Ser. No. 11/124,247, filed May 6, 2005, now U.S. Pat. No. 7,427,551 which is a divisional of U.S. application Ser. No. 10/707,863 filed Jan. 19, 2004, now U.S. Pat. No. 6,969,903.

BACKGROUND OF INVENTION

1. Field of the Invention

The present invention relates to semiconductor devices and methods of manufacturing thereof, and more particularly to a semiconductor resistor structure optimized for tolerance and high current and a method of fabrication thereof. More specifically, the present invention provides a high tolerance Temperature Coefficient of Resistance (TCR) balanced high current resistor for RF CMOS and RE SiGe BICMOS applications and a computer aided design kit for designing the same.

2. Background of the Invention

Optimization of passive elements for tolerance and high current is valuable for RF technologies. In RF circuit applications, precision resistors are needed for I/O circuitry implementing both radio frequency (RF) CMOS an RF SiGe technology. High tolerance resistors are important for accurate prediction of models and statistical control. Moreover, in RF devices and circuits, high tolerance resistors are needed that have good linearity; a low temperature coefficient of resistance (TCR) which is the normalized first derivative of resistance and temperature, and provides an adequate means to measure the performance of a resistor; a high quality factor (Q); and are suitable for high current applications.

In high current RF applications, it is desirable that resistors maintain their structural integrity at high currents. In current multiple inter-level dielectric film stack structures, there exist materials with potentially different thermal and mechanical properties which can influence the temperature distribution within the resistor element and also the mechanical stress and strain in metal and insulation regions. Conventional metal resistor structures subjected to high currents above a critical current-to-failure point, can result in metal blistering, extrusion, and melting of the metal resistor regions. Additionally, subjecting a conventional resistor to high current may result in a thermal gradient in the surrounding insulator that may exceed the yield stress and result in insulator cracking. The above phenomena both reduce the integrity of the dielectric and semiconductor chips when subjected to high current.

Further, in RF CMOS, or RF SiGe, the usage of resistors in series with RF MOSFETs for resistor ballasting in source, drain, and gate regions are valuable for ESD protection. For an RF MOSFET, series resistance is important to minimize for RE performance. Hence, having a low resistance in the source and the drain are important for good RF characteristics. Source and drain resistance are lowered using salicide regions on the source and drain diffusion regions, but salicide near the gate impacts the ESD robustness of the device. For an RF MOSFET device, it is key to provide ballasting effects as well as low resistance. Adding extra resistor elements increase the loading capacitance on the circuit and impacts

area. Hence, finding a means to provide low resistance for RE functionality but ballasting for ESD robustness is key to providing a good RF MOSFET.

It is also well known that current drive in devices at high current is not uniform, largely due to non-uniform temperature distribution in such devices when driven at high currents. Thus, to provide uniformity of current drive, a device which has a more uniform current distribution as a function of device dimensions is an advantage.

Moreover, for RF bipolar and SiGe transistors, a means for establishing uniform current in a transistor to maximize its high current capability is key for power amplifier applications, ESD networks and other applications. Current uniformity can lead to an improved net performance by avoiding increasing a structure size to provide an equivalent drive strength. Additionally, using resistor ballasting in a base region can lead to uniformity of input current. Additionally, using a resistor ballasting in an emitter structure can provide both thermal and electrical stability in a circuit. Additionally, it is important that the element does not structurally fail due to high currents. For differential circuits, it is important that good matching characteristics are present in the physical elements.

It would therefore be highly desirable to provide a semiconductor resistor structure and method of fabrication that is customized to achieve a desired (optimized) TCR, and preferably, a low net Temperature Coefficient of Resistance (TCR) value at high currents and in a joule-heating regime of operation. To this end, it would be desirable to provide a semiconductor resistor element structure and method of fabrication for power amplifiers, and ESD applications that provides a tunable Temperature Coefficient of Resistance for circuit linearity.

It would furthermore be highly desirable to provide a semiconductor resistor element structure and method of fabrication, wherein the resistor element is capable of carrying high currents without failure, and is designed to exhibit internal self-resistor ballasting to maintain a uniform current density and thermal gradient for uniform current distribution and minimization of thermal stress.

It would moreover be highly desirable to provide a semiconductor RF MOSFET device implementing a high resistance element that is physically small, provides a high Q factor, and renders the device electrically and thermally stable at high temperatures and high currents.

ESD protection circuits for input nodes must also support quality de, ac, and RF model capability in order to co-design ESD circuits for analog and RF circuits. With the growth of the high-speed data rate transmission, optical interconnect, wireless and wired marketplaces, the breadth of applications and requirements is broad. Each type of application space has a wide range of power supply conditions, number of independent power domains, and circuit performance objectives. As a result, an ESD design system which has dc and RF characterized models, design flexibility, automation, ESD characterization, and satisfies digital, analog and RF circuits is required to design and co-synthesize ESD needs of mixed signal RF technology.

The ability to design a resistor element so that co-synthesis of the ESD and the functional RF needs to insure integrity of the resistor element is critical in future technologies.

Much effort has been expended by industry to protect electronic devices from ESD damage. Traditionally, ESD designs are custom designed using graphical systems. ESD ground rules and structures are typically built into the designs requiring a custom layout. This has lead to custom design for digital products such as DRAMs, SRAMs, microprocessors, ASIC